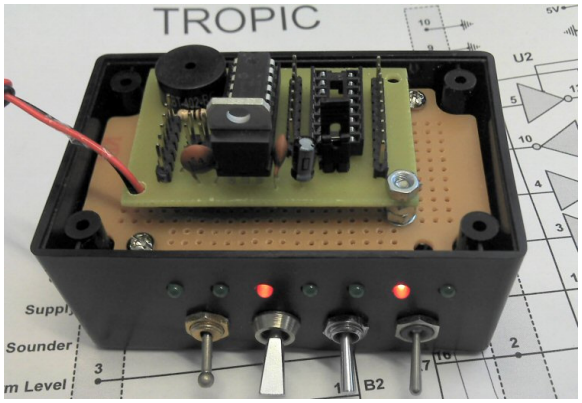
TROPIC

Transmit / Receive Organiser using PIC

Information Manual Version 1.1.0

This manual refers to TROPIC PCB version 1.1



TROPIC prototype during testing

This is a fully supported project.

Please contact gw4gte@s9plus.com *or* GW8LJJ@eddy11.fsnet.co.uk *with any questions, problems or comments before, during or after construction.*

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1. Introduction

TROPIC is a PIC based sequencer designed primarily for amateur radio applications where timed sequential switching is required. Applications typically include correct sequencing of transmit / receive systems to prevent equipment damage, and start-up control of systems where voltages need to be applied in the correct sequence. There are five separate output lines.

The design has been kept simple but flexible. Interfacing to the target system is straightforward. All control outputs are buffered via drivers which can power external relays for total isolation if needed.

The unit can be operated in basic mode, essentially just trigger the PTT line and the outputs activate in sequence. Release the PTT and the outputs de-activate in reverse sequence.

In addition to basic mode, by using the enable input and the two interlock inputs a more elaborate system can be configured whereby dependencies offer an additional level of control and safety.

2. Specification

Output lines ……	5
Output type ……	Buffered, non-isolated, open collector, active low. Suitable for relay drive
Interlock lines ……..……	3 (including PTT enable line)
Triggering ……..	PTT and enable inputs pulled low.
Supply voltage ……	5V direct or 7V to 15V via 5V regulator
Supply current ……..	20mA not including any driver loads.
Sequence Timing ……	25ms, 50ms, 100ms or 200ms selectable via two links
Modes ……	Alarm Mode or Delay Mode (see description)
Alarm indication .....…	PCB mounted transducer plus logic high output line

3. Circuit Description

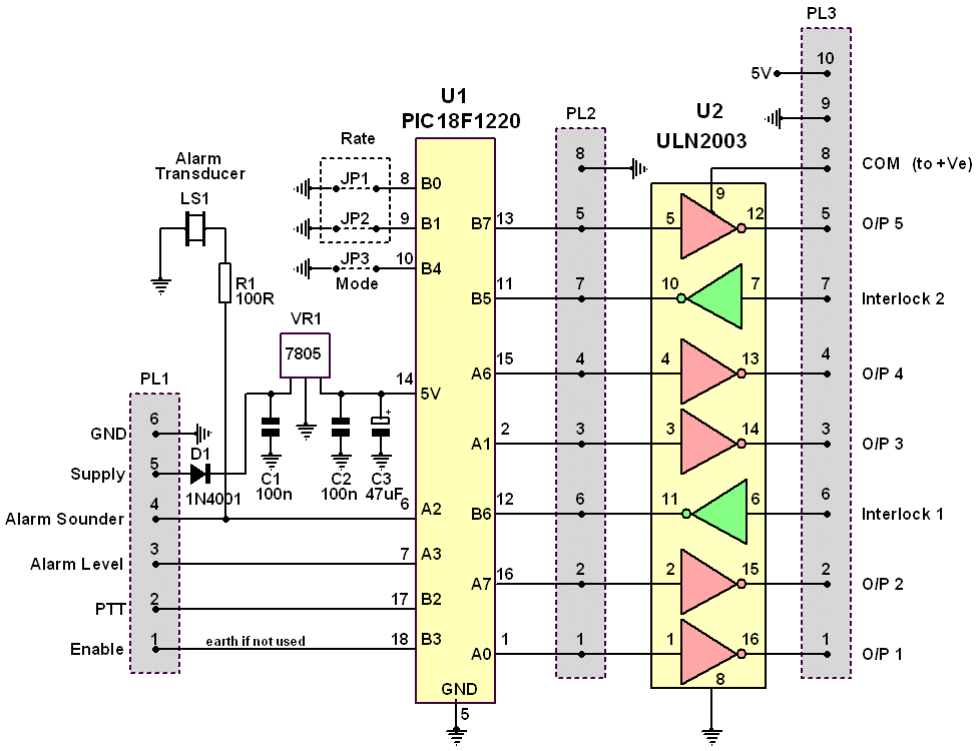

Figure 3.1 TROPIC circuit diagram

Circuit Details

The heart of TROPIC is the PIC processor U1. This chip contains program code that continuously checks the PTT, enable and interlock lines, producing a series of time-sequenced outputs that can be used to control systems where actions are required to happen in a set order, for instance activating an antenna changeover relay before enabling a transmitter. Additionally links JP1 and JP2 control the sequencing speed. These links together with the multiple outputs allow a wide range of speed settings to be configured. JP3 selects one of two modes of operation, described in detail below.

Alarm conditions are reported via the PCB mounted transducer LS1 and a steady logic 1 from the 'alarm level' output.

For simple sequencing requirements many of the functions will not be required. These can be ignored and the unit treated as a basic sequencer.

U2 is a 7 section open collector driver chip, ULN2003. The sections used as outputs (O/P1~O/P5) are driven directly from the PIC output ports. The sections used as interlock inputs are driven from external devices or voltage levels. Unconnected interlock inputs are at logic 0, producing a logic 1 at the PIC. PL2 and PL3 allow connection of additional circuitry. If PL2 is not required it may be omitted from the PCB.

The PTT and enable lines sit at logic 1 when unconnected, and are activated by pulling down to zero volts, usually by means of toggle switches.

Alarm Indication

A PCB mounted sounder provides an audible alarm. This can be placed remotely using PL1/4. an attached alarm LED will flash if connected to PL1/4 via a suitable resistor. In addition PL1/3 provides a steady logic 1 when TROPIC is in alarm mode. This can be used for integrating TROPIC with other components of a control system.

4. Basic Operation

Summary: PTT and Enable inputs are active-low. With no connection they float high via pull-up resistors inside the PIC. Outputs are open-collector with emitters connected to 0V. Interlocks are active-high. With no connection they float low via resistors inside the ULN2003 chip.

For many applications a simple two or three stage sequencer is all that is required. This can be achieved using just the PTT, enable, and one or more output lines. Interlocks 1 and 2 should be left unconnected. If the enable line is not used it needs to be connected to ground (logic 0) so that control is via the PTT alone. See the truth table below.

PTT	Enable	State	O/P1~O/P5
1	1	standby	o/c
0	1	alarm	o/c
1	0	armed	o/c
0	0	activate	activate in sequence

Table 4.1a Truth table to instigate the sequence

Once output sequencing is complete:

PTT	Enable	State	O/P1~O/P5
0	0	active	maintain active
0	1	alarm	maintain active
1	0	de-activate	de-activate in sequence
1	1	standby	o/c

Table 4.1b Truth table to restore outputs to standby

Sequencing speed
This is controlled by jumpers JP1 and JP2. The links may be altered at any time without needing to power down. One of four speeds can be selected. This speed defines the delay between successive O/P lines. O/P1 is activated immediately after a valid activate condition is detected.

JP2	JP1	Speed ms
0	0	25
0	1	50
1	0	200*
1	1	100*

* This is the correct way round. With no links connected, JP1 and JP2 float high, selecting the default 100ms delay.

The position of JP3 is not relevant for basic operation.

5. Interlocks

Note : If only a basic sequencing operation is required, the operation of the interlocks can be ignored. Simply leave the interlock inputs unconnected.

5.1 Alarm mode

Alarm mode is selected when JP3 is unconnected.

Alarm mode resets the sequence if an interlock is activated. Uses are many. For instance a confidence relay in parallel with an antenna changeover relay could be connected to an interlock input, creating an alarm if it fails to operate, or a drive level could be required to be present before the sequencer activates main HT.

For the sequence to complete without entering alarm mode both interlock inputs need to be at logic 0. e.g. interlock 2 needs to be at logic 0 x ms after output 4 is activated, where x = sequence speed selected by JP1/JP2. If an interlock is high when it should be low a return to the standby state will occur by de-activating the outputs in reverse order. Once the sequence has completed, should either interlock go high, alarm mode will also be entered and the outputs sequentially reset in reverse order. The alarm sounder will beep once every 600ms approx to indicate interlock 1 caused the problem, or twice in succession, repeated every 600ms if the problem was interlock 2. If both interlocks are at fault, the sounder beeps 3 times in quick succession. This is repeated until the PTT line goes high whereupon the alarm mode will be cleared.

5.2 Delay mode

Delay mode is selected when JP3 is connected.

Delay mode holds the sequence if an interlock is activated. This is a useful alternative to alarm mode where the precise response of the interlock level is not known but the fastest sequence time is required. However, once the sequence has completed any interlock exception will trigger an alarm as in alarm mode.

For the sequence to complete without entering a sequence hold, both interlock inputs need to be at logic 0. e.g. interlock 2 needs to be at logic 0 x ms after output 4 is activated, where x = sequence speed selected by JP1/JP2. If an interlock is high when it should be low the sequence halts at the interlock and no further outputs are activated until the relevant interlock input goes to zero. TROPIC will stay in this state until PTT is released. No alarm will sound during the halt. Once the sequence has completed however, should either interlock go high, alarm mode will be entered as described below

The alarm sounder will beep once every 600ms approx to indicate interlock 1 caused the problem, or twice in succession, repeated every 600ms if the problem was interlock 2. If both interlocks are at fault, the sounder beeps 3 times in quick succession. This is repeated until the PTT line goes high whereupon the alarm mode will be cleared.

PTT and Enable inputs (both active-low)

Table 4.1 above illustrates the relationship between the PTT and enable inputs. Both need to be active (i.e. low) for the sequence to start. If you only plan to use the PTT line then connect the Enable line to 0V.

The enable line can also be used as a third interlock line or alarm line:
If enable is high when PTT goes low, the alarm beeper sounds and the sequence won't start, so for instance, feed a signal from circuitry that confirms the correct antenna is selected.

If the enable line goes high during a sequenced activation the alarm beeper will sound but the outputs will stay active, so for instance feed in a signal indicating PA temperature climbing.

6. Interfacing

Interfacing at TTL level can be achieved via PL2 and if that is all that is required, U2 can be omitted. Connection to U2 is via PL3. Each U2 channel has a CMOS/TTL compatible input and an open collector output. The circuit in figure 6.1 below is taken from the ULN2003 datasheet.

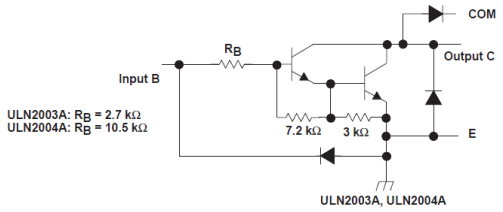

Figure 6.1. Internal circuit of each ULN2003 channel

Input current is around 1mA, and the output transistor can sink around 500mA (single channel used). The COM line is common to all channels. This should be connected to +Ve not earth. It is useful for damping the back emf when used with inductive loads such as relays. Unconnected inputs float low. Unconnected outputs are floating when inactive, and connected to 0V when active.

A typical application could be the sequencing of several stages involved in transceive operation in a home-brew set-up, incorporating safeguards for high VSWR and low TX power. Varying levels such as VSWR can be first fed via an adjustable comparator so the trigger level can be preset before applying to U2. Contact the author for more details. Other inputs could be an "HT fail" line, a PA over-current line or an over-temperature line.

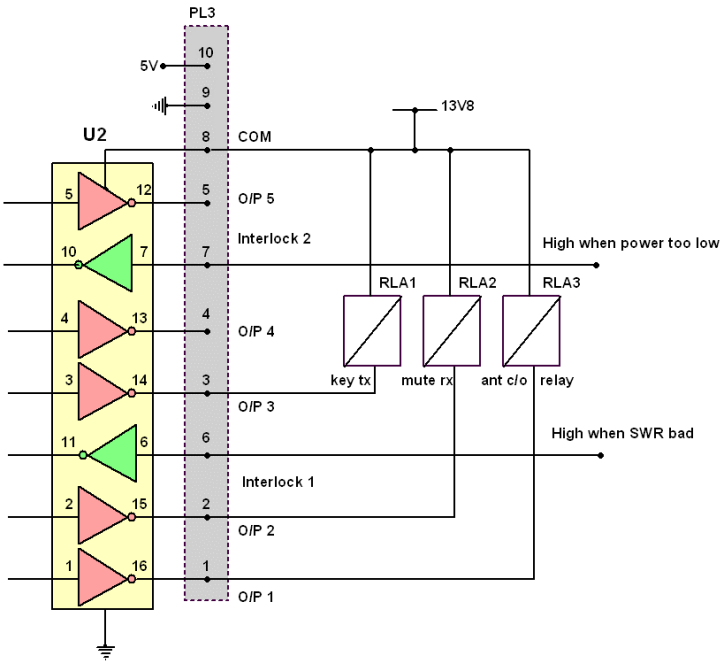

Figure 6.2. Application example.

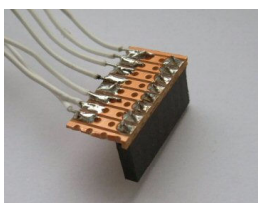

Figure 6.3. Low cost connection method using vero off-cut.

7. Construction

With reference to board layout and parts list below, assemble the supplied parts as shown. Solder the IC sockets first taking care with orientation.

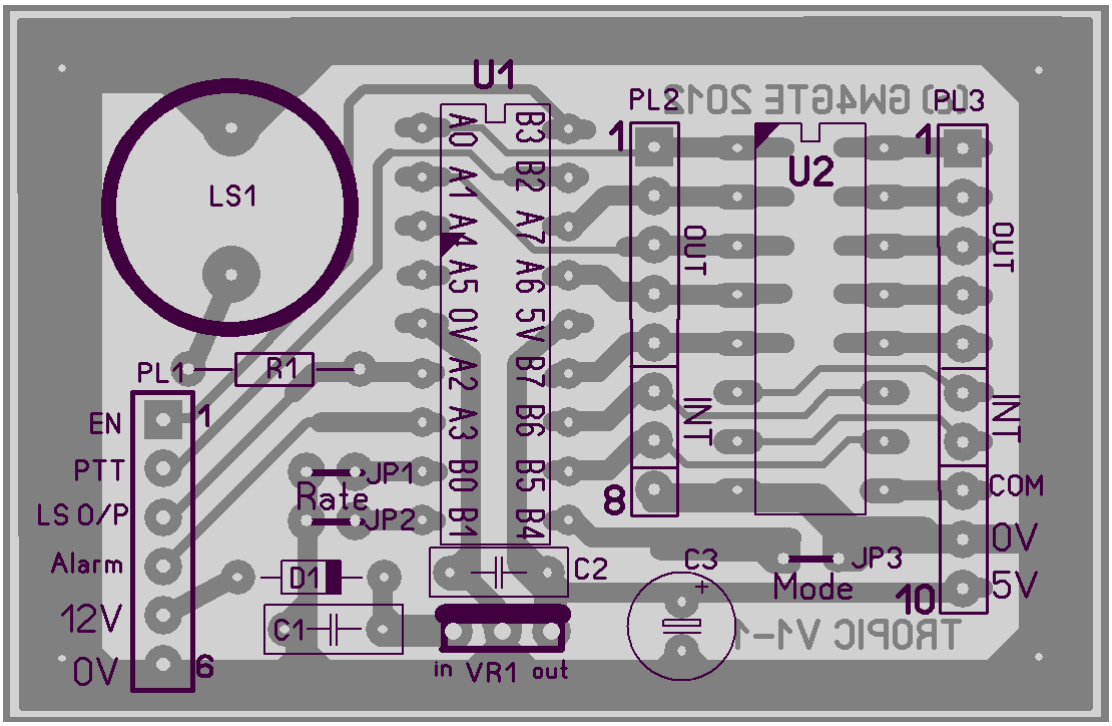

Figure 7.1 Board layout

Part reference	Value	Comments
R1	100R	or s.o.t.
C1	100n	'104'
C2	100n	'104'
C3	47uF	
D1	1N4001	or similar
U1	PIC18F1220	
U2	ULN2003	
VR1	7805	5V reg.
PL1	6 pin header	Control
PL2	10pin header	I/O logic level
PL3	10pin header	I/O via driver
LS1	transducer	
JP1~3	2 pin header	config. links
Skt1	18pin	for U1
Skt2	16 pin	for U2

Table 7.1. Parts list

8. Testing

After construction, carefully check the PCB for solder bridges, particularly under U2 socket. Before inserting U1 and U2, apply 13.8V (or your chosen working voltage) to PL1 and check VR1 is supplying 5V to U1. If all is ok, remove the voltage and insert U1 and U2, being careful to ensure correct orientation.

Switch on again. If LS1 is connected you should hear three short beeps indicating TROPIC has started correctly. Otherwise check PL1/3 'alarm level' which should indicate 5V for 600ms after power-up then revert to 0V.

Refer to table 4.1 and use the PTT and Enable inputs to test each state.

Vary the sequencing speed with JP1 and JP2. Test each interlock mode using JP3.

The outputs can be tested with a multimeter set to ohms. (don't expect a zero ohms reading)

If the above checks fail and there is no obvious reason please contact the author for assistance.

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